# BENTIAN JIANG

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Department of Computer Science & Engineering ⋄ The Chinese University of Hong Kong

## RESEARCH INTERESTS

- Logic synthesis & computer arithmetic (datapath)
- Physical design & design for manufacturability

## EDUCATION

**The Chinese University of Hong Kong, NT, Hong Kong SAR** Aug. 2017 – July 2021
Ph.D., Department of Computer Science & Engineering
Dissertation: "Towards Automated End-to-end VLSI Design for Manufacturability Solutions"
Advisor: Prof. Evangeline F.Y. Young
(CSRankings: CUHK CSE ranked **1st** in the field of Design Automation)

**Sichuan University, Chengdu, P.R. China** Sep. 2013 – Jul. 2017
B.Eng., Electronic & Information Engineering
Dissertation: "Extreme Bilinear Learning Machine for Lithography Hotspot Detection"
Advisor: Prof. Dahai Li

## EXPERIENCES

Principal Engineer | Huawei Hong Kong Research Center April 2022 – Present, Hong Kong SAR

- Design Automation Lab
- Logic synthesis, computer arithmetic (datapath)

* Awardee of *Individual Golden Medal Award* (Highest individual award, Top 1%, 4 out of 400+ employees)

Software Engineer Intern | Cadence Design Systems Inc. April 2019 – Sept. 2019, Austin, TX, USA

- Innovus Clock Tree Synthesis Team
- 3 asscoiated US patents
- Advisor: Dr. Natarajan Viswanathan

Research Assistant | The Chinese University of Hong Kong Mar 2017 – May 2017, Hong Kong SAR

- Bilinear Learning Machine for Lithography Hotspot Detection
- Advisor: Prof. Evangeline F.Y. Young

## SELECTED AWARDS AND HONORS

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|---|---|---|
| **Individual Golden Medal Award** (**Top 1%**, 4 out of 400+) | Huawei Tech. | 2023 |
| The Hong Kong, China - Asia-Pacific Economic Cooperation Scholarship | HKSAR | 2021 |
| Talent Development Scholarship | HKSAR GSF | 2021 |
| DAC Young Fellow Award | DAC | 2020 |
| First Place Award at Contest on Wafer-Scale Deep Learning Accelerator Placement (Leader) | ISPD | 2020 |
| First Place Award at Contest on Initial Detailed Routing | ISPD | 2019 |
| Second Place Award at Contest on Timing-aware Dummy Fill Insertion (Leader) | ICCAD | 2018 |
| Second Place Award at Contest on Initial Detailed Routing | ISPD | 2018 |
| Full Postgraduate Studentship | CUHK | 2017-2021 |
| Outstanding graduate | SCU | 2017 |

## PUBLICATIONS

**Summary**

US patents (3), IEEE TCAD (CCF-A, 4), DAC (CCF-A, 4), ICCAD (CCF-B, 3), ASP-DAC (CCF-C, 1), etc.

**Journal Papers**

[J4] Lixin Liu, Tianji Liu, **Bentian Jiang**, Evangeline FY Young, "Parmesan: Efficient Partitioning and Mapping Flow for DNN Training on General Device Topology", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A, top journal in EDA).

[J3] **Bentian Jiang**, Xinshi Zang, Martin D.F. Wong and Evangeline F.Y. Young, "Exploring Rule-free Layout Decomposition via Deep Reinforcement Learning", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A, top journal in EDA), Volume: 42, Issue: 9, September 2023.

[J2] **Bentian Jiang**, Lixin Liu, Yuzhe Ma, Bei Yu and Evangeline F.Y. Young, "Neural-ILT 2.0: Migrating ILT to Domain-specific and Multi-task-enabled Neural Network", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A, top journal in EDA), Volume: 41, Issue: 8, August 2022.

[J1] **Bentian Jiang***, Jingsong Chen*, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang and Evangeline F.Y. Young, "CU.POKer: Placing DNNs on WSE with Optimal Kernel Sizing and Efficient Protocol Optimization" (* indicates co-first authors), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A, top journal in EDA), Volume: 41, Issue: 6, June 2022.

**Conference Proceedings**

[C10] Shiju Lin, **Bentian Jiang**, Weihua Sheng and Evangeline Young, "Size-Optimized Depth-Constrained Large Parallel Prefix Circuits", ACM/IEEE Design Automation Conference (**DAC**, CCF-A, top conference in EDA), San Francisco, CA, USA, June 23-27, 2024.

[C9] Qijing Wang, **Bentian Jiang**, Martin D.F. Wong and Evangeline F.Y. Young, "A2-ILT: GPU Accelerated ILT with Spatial Attention Mechanism", ACM/IEEE Design Automation Conference (**DAC**, CCF-A, top conference in EDA), San Francisco, CA, USA, Jul. 10-14, 2022.

[C8] Jinwei Liu, Xiaopeng Zhang, Shiju Lin, Xinshi Zang, Jingsong Chen, **Bentian Jiang**, Martin D.F. Wong and Evangeline F.Y. Young, "Partition and Place Finite Element Model on Wafer Scale Engine", ACM/IEEE Design Automation Conference (**DAC**, CCF-A, top conference in EDA), San Francisco, CA, Jul. 10-14, 2022.

[C7] **Bentian Jiang**, Xiaopeng Zhang, Lixin Liu and Evangeline F.Y. Young, "Building up End-to-end Mask Optimization Framework with Self-training", ACM International Symposium on Physical Design (**ISPD**, CCF-C), Virtual Conference, March 21-24, 2021.

[C6] **Bentian Jiang**, Lixin Liu, Yuzhe Ma, Hang Zhang, Bei Yu and Evangeline F.Y. Young, "Neural-ILT: Migrating ILT to Neural Networks for Mask Printability and Complexity Co-optimization, The 39th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B, top conference in EDA), San Diego, CA, USA, Nov. 2-5, 2020.

[C5] **Bentian Jiang***, Jingsong Chen*, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang, Evangeline F.Y. Young, "CU.POKer: Placing DNNs on Wafer-Scale AI Accelerator with Optimal Kernel Sizing", The 39th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B, top conference in EDA), San Diego, CA, USA, Nov. 2-5, 2020 (* indicates co-first authors).

[C4] Haocheng Li, Gengjie Chen, **Bentian Jiang**, Jingsong Chen, and Evangeline F.Y. Young, "Dr. CU 2.0: A Scalable Detailed Routing Framework with Correct-by-Construction Design Rule Satisfaction", The 38th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B, top conference in EDA), Westminster, CO, USA, Nov. 4-7, 2019.

[C3] **Bentian Jiang**, Xiaopeng Zhang, Ran Chen, Gengjie Chen, Peishan Tu, Evangeline F.Y. Young and Bei Yu, "FIT: Fill Insertion Considering Timing", The 57th ACM/IEEE Design Automation Conference (**DAC**, CCF-A, top conference in EDA), Las Vegas, NV, USA, June 2-6, 2019.

[C2] Gengjie Chen, Chak-Wa Pui, Haocheng Li, Jingsong Chen, **Bentian Jiang**, Evangeline F.Y. Young, "Dr. CU: Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search", IEEE/ACM Asia and South Pacific Design Automation Conference (**ASP-DAC**, CCF-C), Tokyo, Japan, Jan 21-24, 2019.

[C1] **Bentian Jiang**, Hang Zhang, Jinglei Yang and Evangeline F.Y. Young, "A Fast Machine Learning-based Mask Printability Predictor for OPC Acceleration", IEEE/ACM Asia and South Pacific Design Automation Conference (**ASP-DAC**, CCF-C), Tokyo, Japan, Jan 21-24, 2019.

**Patents**

[P2] **Bentian Jiang**, Natarajan Viswanathan, Zhuo Li, Yi-Xiao Ding, "Machine-learning based clustering for clock tree synthesis." U.S. Patent 11,645,441, issued May 089, 2023..

[P2] **Bentian Jiang**, Natarajan Viswanathan, Zhuo Li and Yi-Xiao Ding, "Machine-learning based prediction method for iterative clustering during clock tree synthesis." U.S. Patent 11,244,099, issued Feb 08, 2022..

[P1] **Bentian Jiang**, Natarajan Viswanathan, William Robert Reece, and Zhuo Li. "Dynamic weighting scheme for local cluster refinement." U.S. Patent 11,188,702, issued Nov 30, 2021.

## RESEARCH EXPERIENCES

- Lithography Hotspot Detection
  - Extreme bilinear learning machine for lithography hotspot detection.
- Initial Detailed Routing
  - Detailed routing by sparse grid graph and minimum-area-captured path search, **1st** place at ISPD contest.
- Timing-aware Dummy Fill Insertion
  - Robust & efficient timing-aware dummy fill insertion engine, **2nd** place award at ICCAD contest.
- Optical Proximity Correction
  - Migrating inverse lithography correction to neural networks for mask printability and complexity co-optimization.
- Wafer-Scale Deep Learning Accelerator Placement
  - Placing DNNs on wafer-scale AI accelerator with optimal kernel sizing, **1st** place at ISPD contest.
- High performance arithmetic circuits design & optimization
  - High-speed low-power datapath design methodology.

## TEACHING

| | |
|---|---|
| Spring 2020 | Computer-aided Design for Very Large Scale Integrated Circuits |
| Fall 2019 | Introduction to Discrete Mathematics and Algorithms |
| Spring 2019 | Computer Principles and C Programming |
| Fall 2018 | Computer Organization |
| Spring 2018 | Problem Solving By Programming |

## PROFESSIONAL SERVICES

**Technical Program Committee Member**

- IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B), 2022

**Journal Reviewer**

- ACM Transaction on Design Automation of Electronic Systems (**TODAES**, CCF-B)
- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A)

**Conference (External) Reviewer**

- ACM/IEEE Design Automation Conference (**DAC**, CCF-A)
- IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B)

## TECHNICAL SKILLS

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|---|---|
| **Languages** | C/C++, Python, CUDA, Tcl, LaTeX |
| **Operating Systems** | Linux/UNIX |
| **Tools** | Synopsys Design Compiler®, Cadence® Genus™, Cadence® Innovus™ |