**Timing Aware Dummy Fill Insertion**

- **Dummy fill insertion**
  - Reduce dielectric thickness variation;
  - Provide near-unity pattern density;
  - Highly-related to the quality of chemical-mechanical polishing (CMP) process.
- **Taming-aware Dummy Fill Insertion**
  - Inserted metal \( \Rightarrow \) Prov: improves density, increases planarity
  - \( \Rightarrow \) Cons: couples with signal tracks
  - \( \Rightarrow \) Severely affect the original layout timing closure.
  - \( \Rightarrow \) Need to reduce the coupling impact during the metal fill insertion.

**Capacitance Evaluation**

- **Area Capacitance**
  - Two conductors on different metal layers, and their projections overlap \( \Rightarrow C^a = P_1(\delta) \times x \).
- **Lateral Capacitance**
  - Two conductors on the same layer and have horizontal overlap \( \Rightarrow C^l = P_2(d) \times l \).
- **Fringe Capacitance**
  - Two conductor pieces on different layers, and have parallel edge overlap \( \Rightarrow C^{fp} = P_3(\delta) \times x \).

**Problem Formulation**

- **Given a design layout**, insert metal fills to minimize:
  - Equivalent capacitance *.
- **Overall runtime**
  - The insertion result must satisfy the hard constraints on:
    - **Density criteria**
      - A running window of size \( w \times w \) and a step size of \( s \) is considered on each layer, the density inside the window cannot violate the given density lower and upper bound.
    - **Design rules**
      - Minimum spacing, minimum fill width, and maximum fill width.

- **Additionally**, the total parasitic capacitance of all the signal nets is also considered, since it will affect the performance like noise consumption, timing.

*Equivalent capacitance is the grade, can be obtained by network analysis methods.

**Overview of FIT Flow**

- **Efficient**: Strong runtime performance on ICCAD 2018 benchmarks.
- **Effective**: Outperforms the contest winner by all metrics.
- **Extendable**: Separate modules, easy to further integrate other optimization flow.

**Figures**

- Overall dummy fill insertion flow.
- Fillable Region Generation.
- Target Density Planning.
- Global Fill Synthesis.
- Detailed Post Refinement.
- Parasitic Extractor and Equivalent Capacitance Calculation.

**Detailed Post Refinement**

- **Taming-aware Fill Relocation**
  - Relocate those fills obtained from GFS with high-impact on timing.

- **Taming-aware Fill Shifting**
  - To capture the lateral and fringe capacitance with respect to critical wires.

  \[
  \min_{n} \sum_{i} \{ \text{area overlap} \} \leq \text{critical wire fill}
  \]

**Experimental Results**

- **On ICCAD 2018 Contest Benchmarks**
  - Capacitance evaluation tool is released by the contest organizers.

**Global Fill Synthesis and Legalization**

- An efficient heuristic window-based flow for high-quality initial solution.
- Guided by the target density scheduling result.
- Only performing the GIF flow can already beat the contest winner results.

**Insertion criteria**

- Increase the spacing and reduce the parallel overlap lengths between any two metal conductors.
- Forbid any area overlap between fill and the given critical wire.
- Order-Sensitive process, obtain a better insertion order:
  - Sort the window order by the density gap \( D_{\text{window}} \).
- Sort the fillable rectangles by weighted score of their shape, area, and distance and parallel overlap to: surrounding critical wires.

\[
\alpha \cdot b + \beta \cdot A + \gamma \cdot \sqrt{D_{\text{window}}} + \delta = \frac{1}{\eta}
\]

**Legalization**

- A design rules checker (RTTmix) is maintained to perform legalization and record density.
- Noise implementation: Insert all wires and fills into checker \( \Rightarrow \) Time consuming.
- Pruning: Global checker \( \Rightarrow \) Local checkers.
- Local checker responsible for insertion and legalization of a specific window, discard when finished.
- Global checker keeps wire locations for the entire layer (or one partitioned region of the layer), success insertion of a window only commits those fills that close to window border to global checker.

**Case Studies**

- Case 1: \( 0.7725 \)
  - Critical wire Fill Block Fillable rectangle Shift region
- Case 2: \( 0.7642 \)
- Case 3: \( 0.7632 \)
- Case 4: \( 0.7196 \)
- Case 5: \( 0.7339 \)

**Fillable Region Generation**

- Extract fillable polygons of the entire design.
- Polygon decomposition: polygons with thousands of vertices and maybe holes inside are difficult to handle \( \Rightarrow \) decompose them to rectangles, assign rectangles into different windows \( \Rightarrow \) Merged fillable region.
- The aspect ratio of rectangle fits the layer preferred direction. Use sweep line to merge rectangles locally.
- Comparing to [Liu+, TODDES’15], significantly expand the solution spaces for later procedures.

**Target Density Planning**

**Objective**

- Distribute the target density for each window (under density constraints).
- Divide original window \( w \times w \) into 2 sub-windows with size of \( \frac{w}{2} \times \frac{w}{2} \).
- Reduce the critical nets capacitance and total capacitance.

\[
\min \sum_{i} \sum_{j} \Delta f_{ij} + \delta m_{\text{total}}(f_{ij} - D_{ij})
\]

**Windows average density upper bound**

- Critical wire Fill Block Fillable rectangle Shift region

**Global Fill Synthesis is very effective, already beats the contest winner.**

**Target density planning and detailed post refinement stages can significantly further reduce critical capacitance.**

**FIT framework outperforms the contest winner in all metrics.**

- **8% reduction** on critical nets capacitance, **2%** reduction on total capacitance of all nets. **2×** runtime speedup in single-thread execution, and **3.3×** in multi-thread execution.

**Table:**

<table>
<thead>
<tr>
<th>Case</th>
<th>Wire</th>
<th>Fillable Region</th>
<th>Critical</th>
<th>Fillable</th>
<th>Shift region</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>2</td>
<td>0.98</td>
<td>0.98</td>
<td>0.98</td>
<td>0.98</td>
<td>0.98</td>
</tr>
<tr>
<td>3</td>
<td>0.96</td>
<td>0.96</td>
<td>0.96</td>
<td>0.96</td>
<td>0.96</td>
</tr>
<tr>
<td>4</td>
<td>0.92</td>
<td>0.92</td>
<td>0.92</td>
<td>0.92</td>
<td>0.92</td>
</tr>
<tr>
<td>5</td>
<td>0.89</td>
<td>0.89</td>
<td>0.89</td>
<td>0.89</td>
<td>0.89</td>
</tr>
</tbody>
</table>

**FIT:** Fill Insertion considering Timing

Bentian Jiang, Xiaopeng Zhang, Ran Chen, Gengjie Chen, Peishan Tu, Wei Li, Evangeline F. Y. Young and Bei Yu

CSE Department, The Chinese University of Hong Kong